EUROPEAN PATENT OFFICE

Patent Abstracts of Japan

PUBLICATION NUMBER : 2003037493
PUBLICATION DATE : 07-02-03

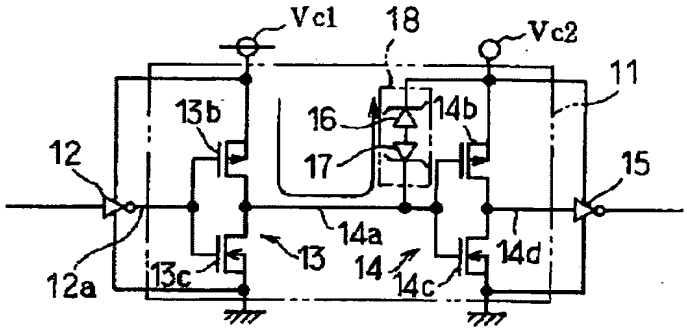
APPLICATION DATE : 23-07-01
APPLICATION NUMBER : 2001221453

APPLICANT : DENSO CORP;

INVENTOR : TOYODA HIROICHI;

INT.CL. : H03K 19/0948 H02H 9/04

TITLE : INTERFACE CIRCUIT



Vc1:第１の電源端子
Vc2:第２の電源端子
13:第１のＣＭＯＳインバータ
14:第２のＣＭＯＳインバータ
18:電圧制限手段

ABSTRACT : PROBLEM TO BE SOLVED: To provide an interface circuit that can eliminate sneak path for a voltage from being produced, even if a voltage difference between two power supplies occurs, while preventing its internal elements due to a surge voltage from breaking down.

SOLUTION: The interface circuit 11 comprises a CMOS inverter 13 that is energized from a power terminal Vc1; a CMOS inverter 14 that is energized from a power terminal Vc2; and two Zener diodes 16, 17 placed between the power terminal Vc2 and an input terminal 14a connected in anti-series. Even if a voltage Vcc1 is applied to the input terminal 14a of the CMOS inverter 14, no power will be supplied to the power terminal Vc2 due to the presence of the Zener diodes 16, 17. Further, even if a surge voltage is applied to the power terminal Vc1, clamp the surge voltage will be clamped by the Zener diodes 16, 17, and a current caused by the surge voltage is led to the power terminal Vc2.